



# 1 pC Charge Injection, 100 pA Leakage, CMOS $\pm 5$ V/+5 V/+3 V Quad SPST Switches

## ADG611/ADG612/ADG613

### FEATURES

- 1 pC Charge Injection
- $\pm 2.7$  V to  $\pm 5.5$  V Dual Supply
- +2.7 V to +5.5 V Single Supply
- Automotive Temperature Range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- 100 pA Max @  $25^{\circ}\text{C}$  Leakage Currents
- 85  $\Omega$  On-Resistance
- Rail-to-Rail Switching Operation
- Fast Switching Times
- 16-Lead TSSOP Packages
- Typical Power Consumption ( $<0.1$   $\mu\text{W}$ )
- TTL/CMOS-Compatible Inputs

### APPLICATIONS

- Automatic Test Equipment
- Data Acquisition Systems
- Battery-Powered Systems
- Communication Systems
- Sample and Hold Systems
- Audio Signal Routing
- Relay Replacement
- Avionics

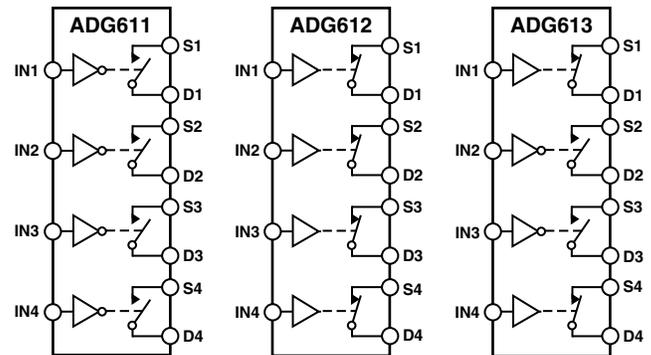
### GENERAL DESCRIPTION

The ADG611, ADG612, and ADG613 are monolithic CMOS devices containing four independently selectable switches. These switches offer ultralow charge injection of 1 pC over full input signal range and typical leakage currents of 10 pA at  $25^{\circ}\text{C}$ .

They are fully specified for  $\pm 5$  V, +5 V, and +3 V supplies. They contain four independent single-pole/single-throw (SPST) switches. The ADG611 and ADG612 differ only in that the digital control logic is inverted. The ADG611 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG612. The ADG613 contains two switches whose digital control logic is similar to the ADG611, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the supplies. The ADG613 exhibits break-before-make switching action. The ADG611/ADG612/ADG613 are available in small 16-lead TSSOP packages.

### FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

### PRODUCT HIGHLIGHTS

1. Ultralow Charge Injection (1 pC typically)
2. Dual  $\pm 2.7$  V to  $\pm 5.5$  V or Single +2.7 V to +5.5 V Operation.
3. Automotive Temperature Range,  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
4. Small 16-lead TSSOP package.

REV. 0

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# ADG611/ADG612/ADG613—SPECIFICATIONS

**DUAL SUPPLY**<sup>1</sup> ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	25°C	Y Version		Unit	Test Conditions/Comments
		-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{SS}$ to $V_{DD}$	V	
On-Resistance ( $R_{ON}$ )	85 115			$\Omega$ typ $\Omega$ max	$V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$ Test Circuit 1
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	2 4	5.5	6.5	$\Omega$ typ $\Omega$ max	$V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	25 40	55	60	$\Omega$ typ $\Omega$ max	$V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$ $\pm 0.1$	$\pm 0.25$	$\pm 2$	nA typ nA max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$ $\pm 0.1$	$\pm 0.25$	$\pm 2$	nA typ nA max	$V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$ $\pm 0.1$	$\pm 0.25$	$\pm 6$	nA typ nA max	$V_D = V_S = \pm 4.5\text{ V}$ , Test Circuit 3
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.4	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	2			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	45 65	75	90	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.0\text{ V}$ , Test Circuit 4
$t_{OFF}$	25 40	45	50	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.0\text{ V}$ , Test Circuit 4
Break-Before-Make Time Delay, $t_D$	15		10	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3.0\text{ V}$ , Test Circuit 5
Charge Injection	-0.5			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 6
Off Isolation	-65			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 7
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 8
-3 dB Bandwidth	680			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	5			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
$I_{SS}$	0.001		1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital Inputs = 0 V or 5.5 V

## NOTES

<sup>1</sup>Temperature range is as follows. Y Version: -40°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**SINGLE SUPPLY<sup>1</sup>** ( $V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	Y Version			Unit	Test Conditions/Comments
	25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On-Resistance ( $R_{ON}$ )	210			$\Omega$ typ	$V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$ ; Test Circuit 1
	290	350	380	$\Omega$ max	
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	3			$\Omega$ typ	$V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$
	10	12	13	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ ; Test Circuit 2
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$			nA typ	$V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ ; Test Circuit 2
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$			nA typ	$V_S = V_D = 1\text{ V}$ or $4.5\text{ V}$ , Test Circuit 3
	$\pm 0.1$	$\pm 0.25$	$\pm 6$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.4	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance <sup>2</sup>	2			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	70			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	100	130	150	ns max	$V_S = 3.0\text{ V}$ , Test Circuit 4
$t_{OFF}$	25			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	40	45	50	ns max	$V_S = 3.0\text{ V}$ , Test Circuit 4
Break-Before-Make Time Delay, $t_D$	25			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = 3.0\text{ V}$ , Test Circuit 5
Charge Injection	1			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 6
Off Isolation	-62			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ Test Circuit 7
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ Test Circuit 8
-3 dB Bandwidth	680			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	5			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
			1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows. Y Version: -40°C to +125°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG611/ADG612/ADG613—SPECIFICATIONS

**SINGLE SUPPLY**<sup>1</sup> ( $V_{DD} = 3\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	Y Version			Unit	Test Conditions/Comments
	25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analogue Signal Range			0 V to $V_{DD}$	V	$V_S = 1.5\text{ V}$ , $I_S = -1\text{ mA}$ ; Test Circuit 1
On-Resistance ( $R_{ON}$ )	380	420	460	$\Omega$ typ	
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = 3.3\text{ V}$ $V_S = 1\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/1\text{ V}$ ; Test Circuit 2 $V_S = 1\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/1\text{ V}$ ; Test Circuit 2 $V_S = V_D = 1\text{ V}$ or $3\text{ V}$ , Test Circuit 3
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$			nA typ	
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$			nA typ	
	$\pm 0.1$	$\pm 0.25$	$\pm 6$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	$V_{IN} = V_{INL}$ or $V_{INH}$
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current					
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2			pF typ	
<b>DYNAMIC CHARACTERISTICS</b> <sup>2</sup>					
$t_{ON}$	130			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$ , Test Circuit 4
	185	230	260	ns max	
$t_{OFF}$	40			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$ , Test Circuit 4
	55	60	65	ns max	
Break-Before-Make Time Delay, $t_D$	50			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = 2\text{ V}$ , Test Circuit 5
Charge Injection	1.5			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 6
Off Isolation	-62			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ Test Circuit 7
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ Test Circuit 8
-3 dB Bandwidth	680			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	5			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001		1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V

## NOTES

<sup>1</sup>Temperature ranges are as follows. Y Version: -40°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG611/ADG612/ADG613

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	13 V
V <sub>DD</sub> to GND .....	-0.3 V to +6.5 V
V <sub>SS</sub> to GND .....	+0.3 V to -6.5 V
Analog Inputs <sup>2</sup> .....	V <sub>SS</sub> - 0.3 V to V <sub>DD</sub> + 0.3 V
Digital Inputs <sup>2</sup> .....	GND - 0.3 V to V <sub>DD</sub> + 0.3 V
Peak Current, S or D .....	20 mA
	(Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D .....	10 mA
3 V operation 85°C to 125°C .....	7.5 mA
Operating Temperature Range	
Automotive (Y Version) .....	-40°C to +125°C

Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	150°C
16-Lead TSSOP, θ <sub>JA</sub> Thermal Impedance .....	150.4°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) .....	215°C
Infrared (15 sec) .....	220°C

### NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overtolerances at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG611YRU	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG612YRU	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG613YRU	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16

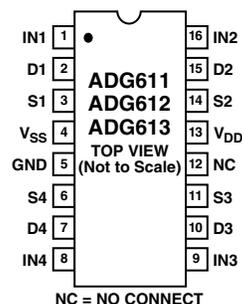
Table I. ADG611/ADG612 Truth Table

ADG611 In	ADG612 In	Switch Condition
0	1	ON
1	0	OFF

Table II. ADG613 Truth Table

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

## PIN CONFIGURATIONS



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG611/ADG612/ADG613 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

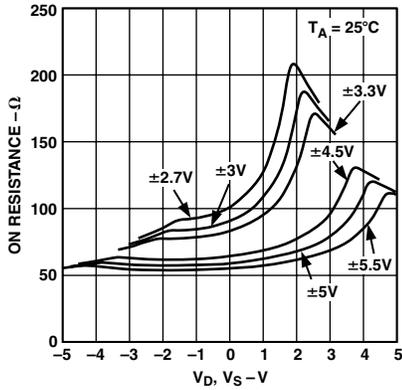


# ADG611/ADG612/ADG613

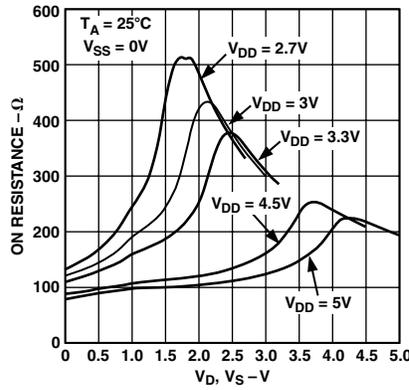
## TERMINOLOGY

$V_{DD}$	Most Positive Power Supply Potential
$V_{SS}$	Most Negative Power Supply Potential
$I_{DD}$	Positive Supply Current
$I_{SS}$	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output
D	Drain Terminal. May be an input or output
IN	Logic Control Input
$V_D (V_S)$	Analog Voltage on Terminals D, S
$R_{ON}$	Ohmic Resistance between D and S
$\Delta R_{ON}$	On Resistance match between any two channels, i.e., $R_{ONMAX} - R_{ONMIN}$ .
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
$I_S$ (OFF)	Source Leakage Current with the Switch “OFF”
$I_D$ (OFF)	Drain Leakage Current with the Switch “OFF”
$I_D, I_S$ (ON)	Channel Leakage Current with the Switch “ON”
$V_{INL}$	Maximum Input Voltage for Logic “0”
$V_{INH}$	Minimum Input Voltage for Logic “1”
$I_{INL}(I_{INH})$	Input Current of the Digital Input.
$C_S$ (OFF)	“OFF” Switch Source Capacitance. Measured with reference to ground.
$C_D$ (OFF)	“OFF” Switch Drain Capacitance. Measured with reference to ground.
$C_D, C_S$ (ON)	“ON” Switch Capacitance. Measured with reference to ground.
$C_{IN}$	Digital Input Capacitance
$t_{ON}$	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
$t_{OFF}$	Delay between applying the digital control input and the output switching off.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
On Response	Frequency Response of the “ON” Switch
Insertion Loss	Loss Due to the ON Resistance of the Switch

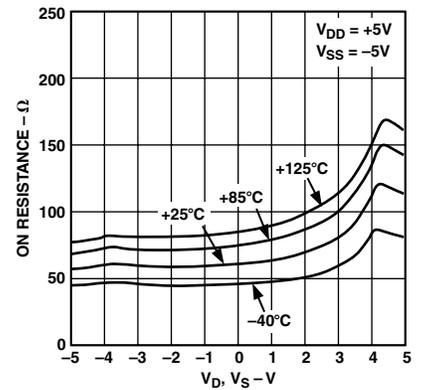
# Typical Performance Characteristics—ADG611/ADG612/ADG613



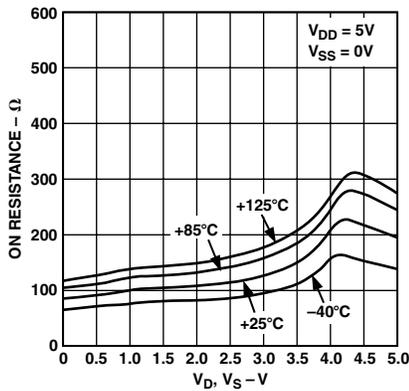
TPC 1. On Resistance vs.  $V_D(V_S)$ , Dual Supply



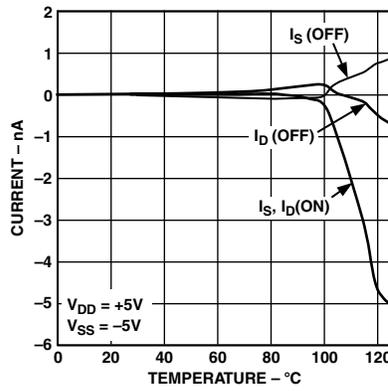
TPC 2. On Resistance vs.  $V_D(V_S)$ , Single Supply



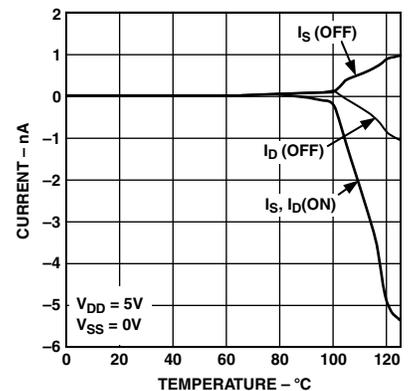
TPC 3. On Resistance vs.  $V_D(V_S)$  for Different Temperatures, Dual Supply



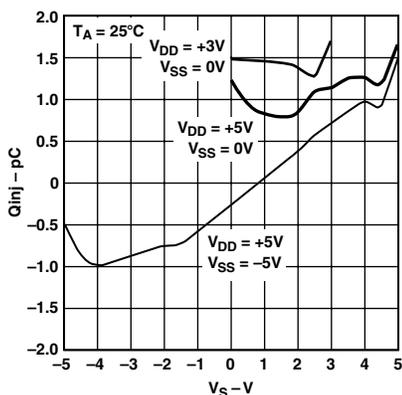
TPC 4. On Resistance vs.  $V_D(V_S)$  for Different Temperatures, Single Supply



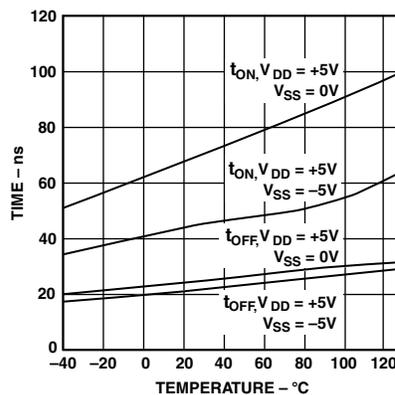
TPC 5. Leakage Currents vs. Temperature, Dual Supply



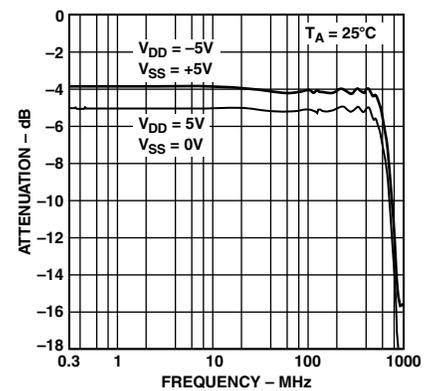
TPC 6. Leakage Currents vs. Temperature, Single Supply



TPC 7. Charge Injection vs. Source Voltage

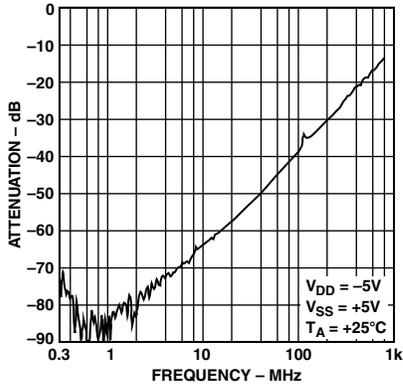


TPC 8.  $t_{ON}/t_{OFF}$  Times vs. Temperature

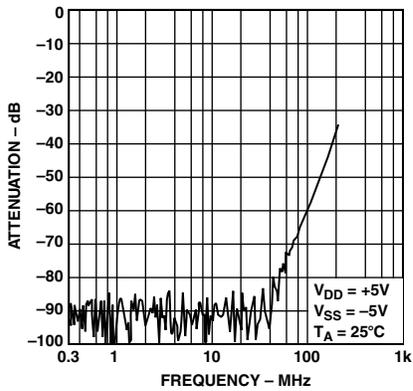


TPC 9. On Response vs. Frequency

# ADG611/ADG612/ADG613



TPC 10. Off Isolation vs. Frequency



TPC 11. Crosstalk vs. Frequency

## APPLICATIONS

Figure 1 illustrates a photodetector circuit with programmable gain. With the resistor values shown in the circuits, and using different combinations of switches, gains in the range of 2 to 16 can be achieved.

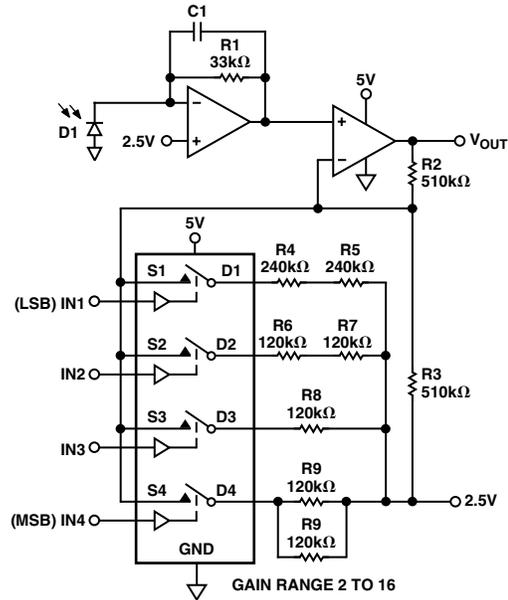
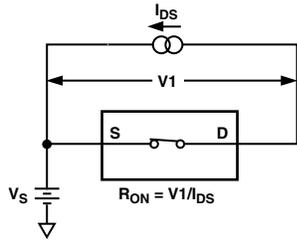
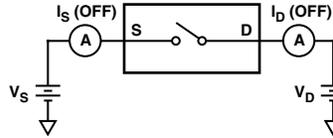


Figure 1. Photodetector Circuit with Programmable Gain

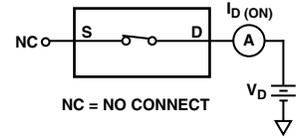
# Test Circuits



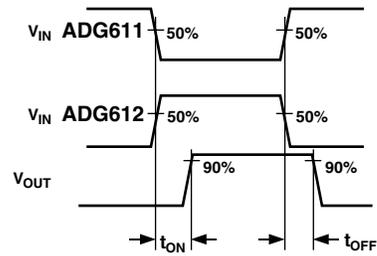
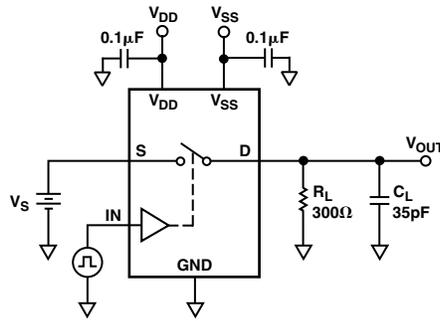
Test Circuit 1. On Resistance



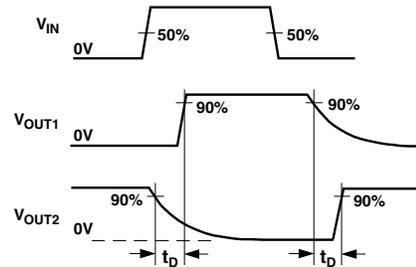
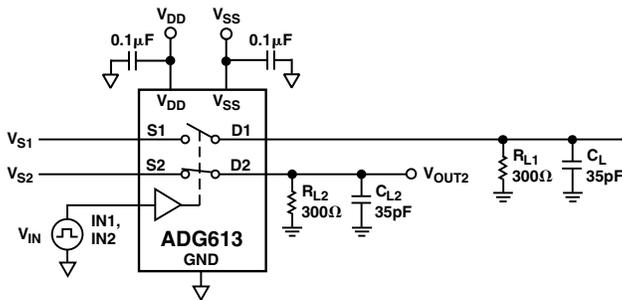
Test Circuit 2. Off Leakage



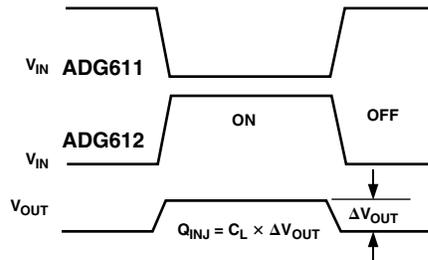
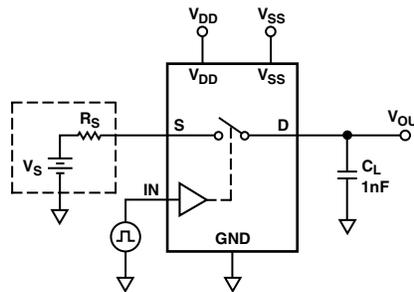
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

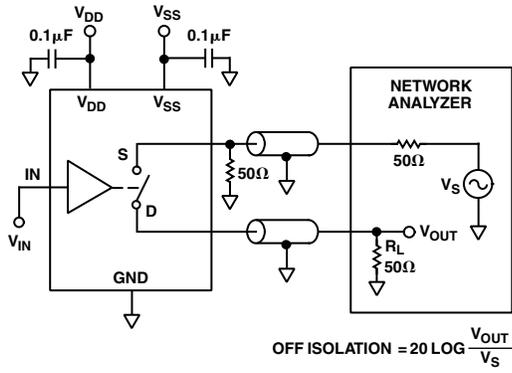


Test Circuit 5. Break-Before-Make Time Delay

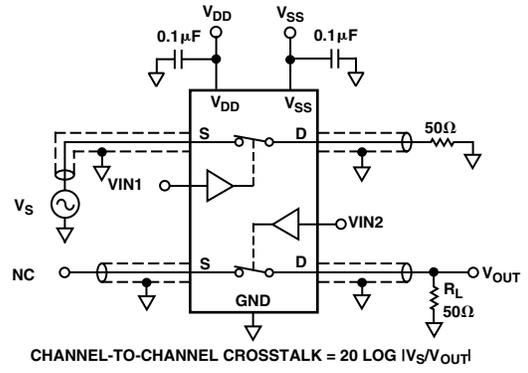


Test Circuit 6. Charge Injection

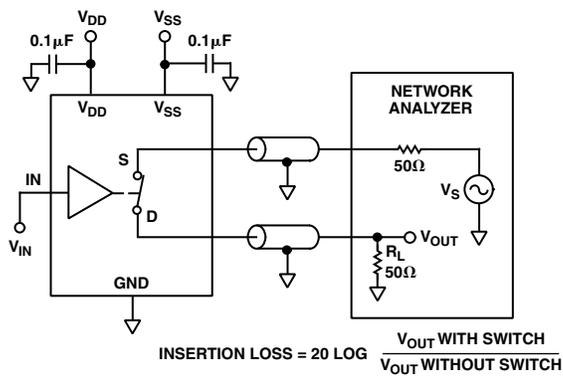
# ADG611/ADG612/ADG613



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk



Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP  
(RU-16)

